CHALLENGES IN MATERIALS AND PROCESSES FOR NEW APPLICATIONS

Laurent Clavelier
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Leti Workshop @ Semicon West | July 10, 2018

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OUTLINE

Challenges in Materials and Processes for New Applications

2 examples to illustrate the way Leti works:

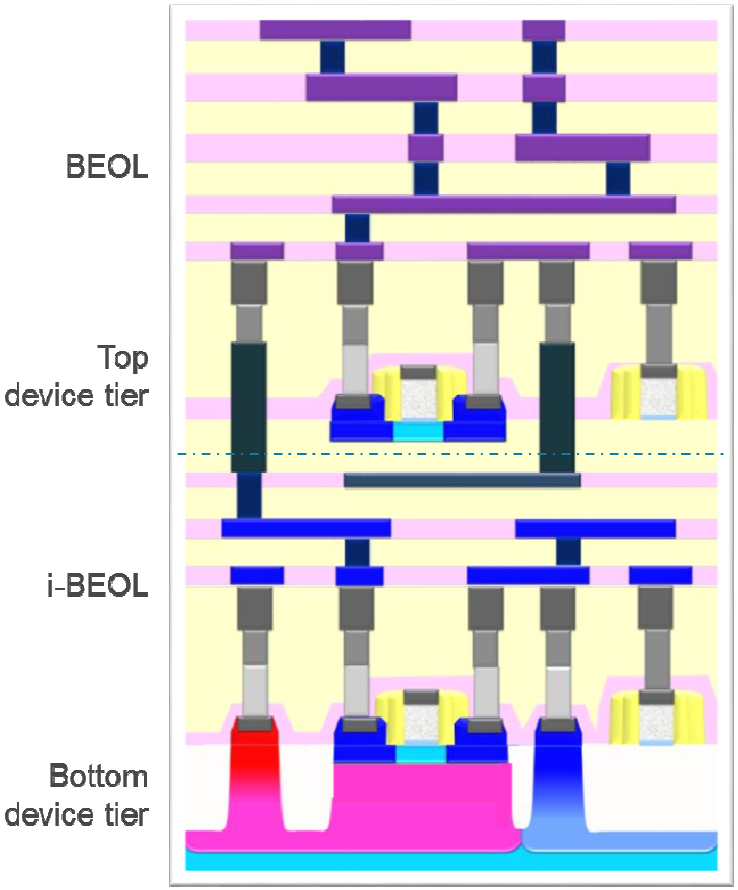
- **More Moore: CoolCube**

How to do sequential stacking for advanced CMOS with molecular bonding and « low Temperature » process bricks

- **More Than Moore : Photonics**

How to manipulate « exotic materials » like silicon and on large diameter substrates

SEQUENTIAL STACKING (COOLCUBE™) INTEGRATION



Kerdiles ECS 2017

Parallel integration (e.g.: TSV)	Sequential integration
3D TSV contact pitch: 3-8µm 3D contact density: 10^4-10^5 /mm²	3D contact pitch: < 100 nm 3D contact density: > 10^8 /mm²
Bonding stepper alignment : ~1µm	Lithography stepper alignment : ~5 nm

Sequential process:

- Classical CMOS process

- Wafer bonding of a blanket wafer w/o alignement (cold smart cut™ process for example)

- Low-temp process (<500℃)

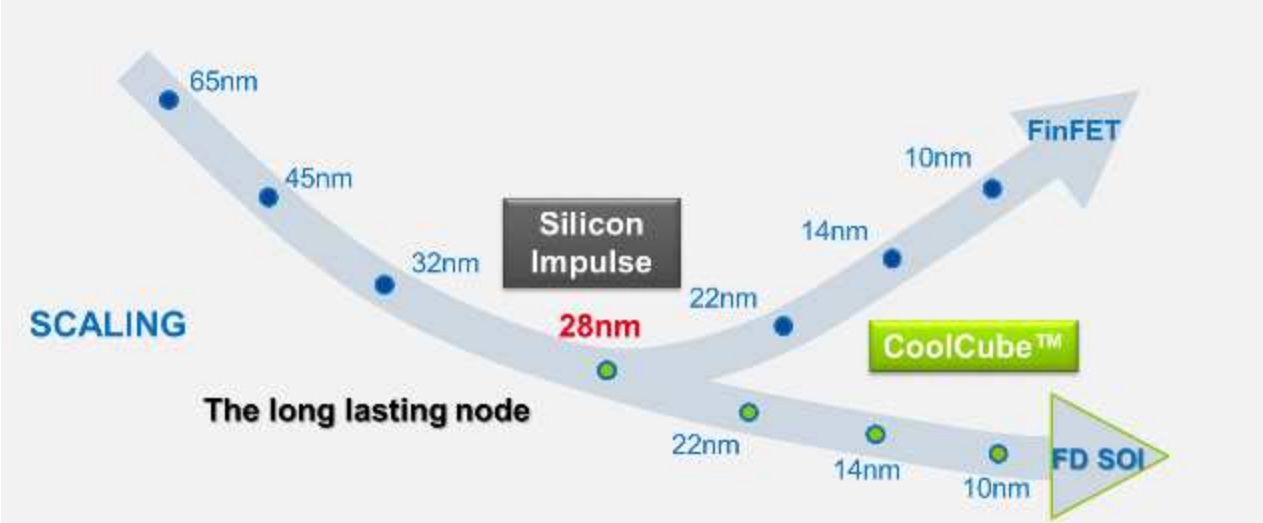
- 3D contacts

Enabling solution for:

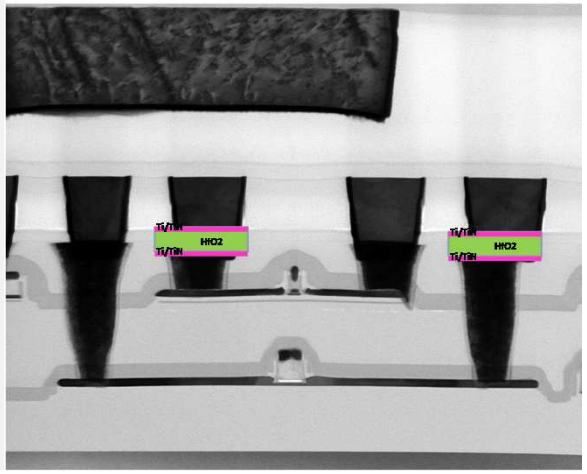
- CMOS on CMOS as a scaling alternative

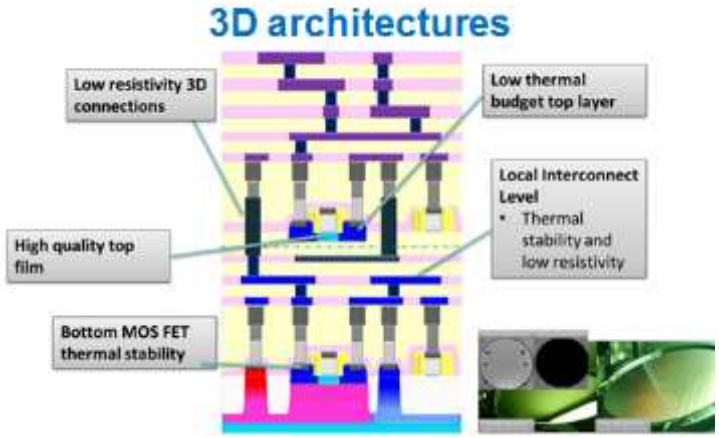
- CMOS on active matrix (LED, Imager, MEMS, …)

SEQUENTIAL STACKING (COOLCUBE™): AN ECONOMICALLY VIABLE ALTERNATIVE TO SLOW DOWN SCALING AND DEVELOP NEW ARCHITECTURES



Neuromorphic computing

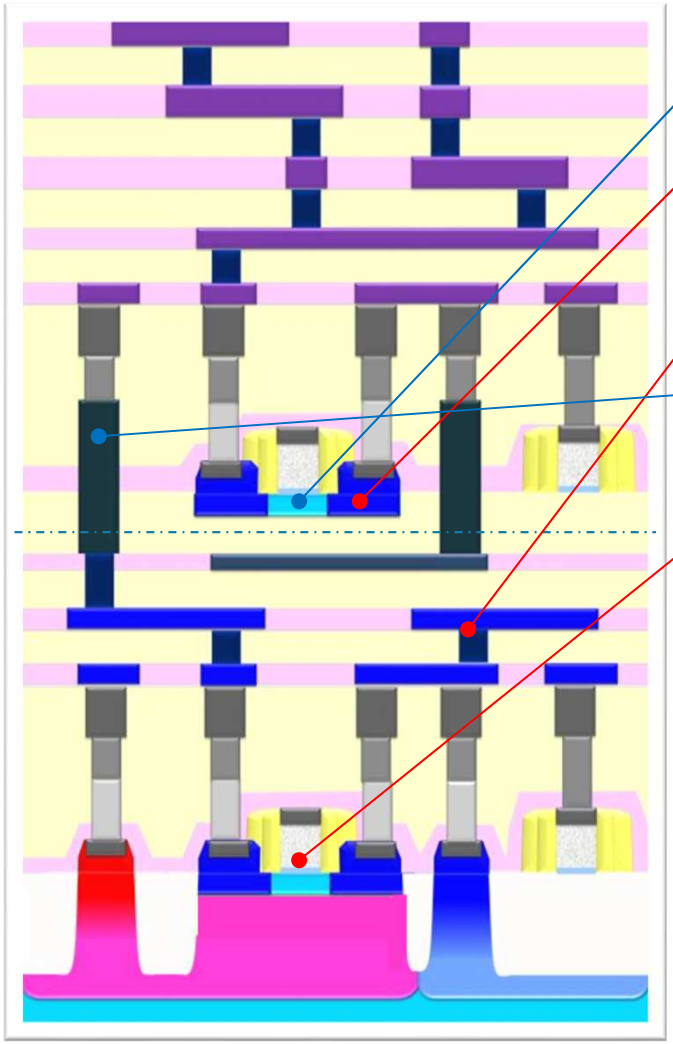




Economics :
- 28nm node
- 40mm² chip
- 5kW/W production (or equivalent surface)

→ 100M$ saving / year (compared to a 28FDSOI) thanks to the additional number of dies provided by the CoolCube™ solution

MAIN COOLCUBE™ INTEGRATION CHALLENGES



High quality top film

« Cold » processing for the top level
Local interconnect level thermal stability and low resistivity

Low resistivity 3D connections

Bottom MOS FET thermal stability

Thermal budget limitation

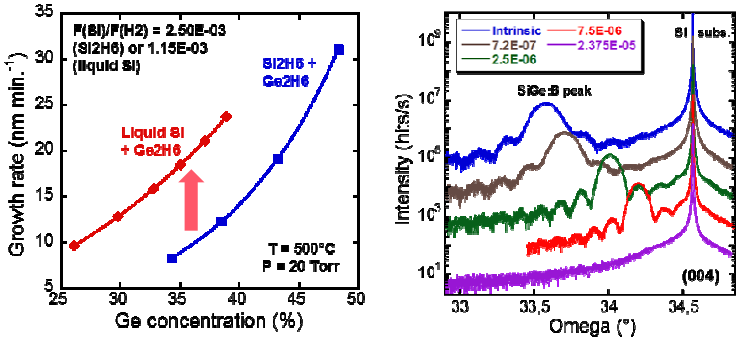
Kerdiles ECS 2017

RECENT DEVELOPMENTS ON LOW TEMPERATURE EPITAXY

- **Si & SiGe:(B) epitaxy from 450 to 550℃**
  - Investigation Liquid silicon as a new precursor

  ⇒ better growth rates vs Si_2H_6 / good crystallinity and surface roughness

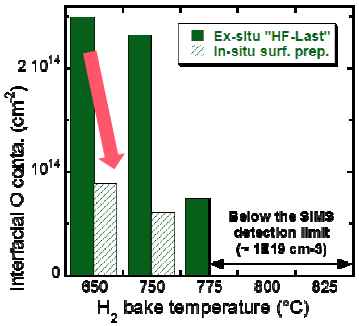
  ⇒ Selective epitaxy under development



V. Mazzocchi *et al*, ECS 2018

- **Surface preparation for low temp epitaxy**
  - *in-situ surface preparation* vs *standard HF last* process

  ⇒ Strong impact on interface oxygen conta. with reduced bake temperature

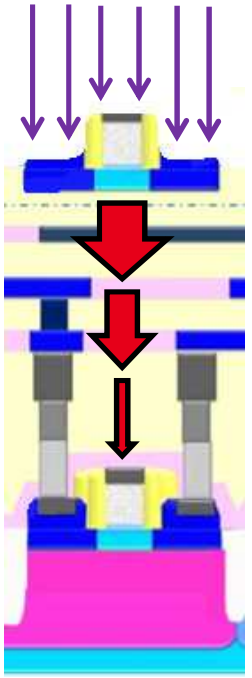


JM Hartmann *et al*, ECS 2018

ALTERNATIVE: SELECTIVE SURFACE ANNEALING

Thermal budget limitation originates from the bottom level, with techniques heating the whole wafer

→ Ultraviolet Nanosecond Laser Annealing

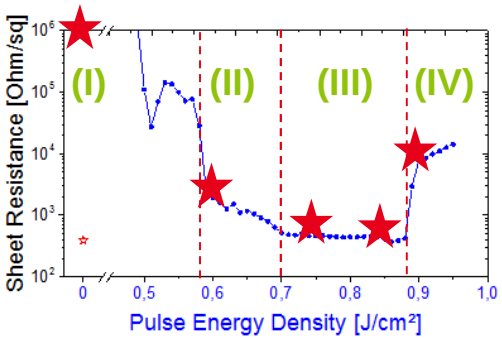


LASSE-SCREEN LT-3100 platform for UV-NLA

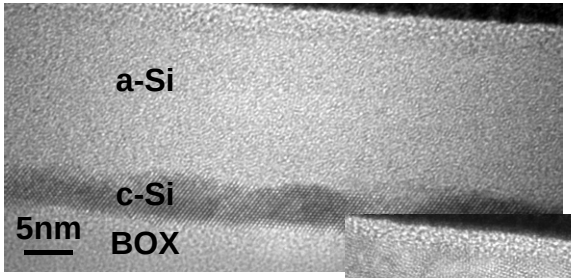
- UV radiation (308nm) : absorption length ~ top Si film thickness (5-20nm)
- Short pulse (< 200ns) : very limited heat diffusion

→ **UV-NLA only heats the top transistor**

MICROSTRUCTURE BY TEM: As IMPL.

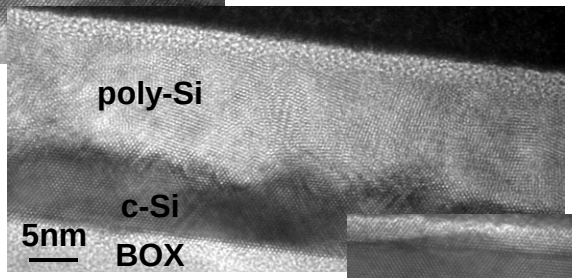


- **As-implanted:** 4-5nm c-Si seed + 14-15nm a-Si

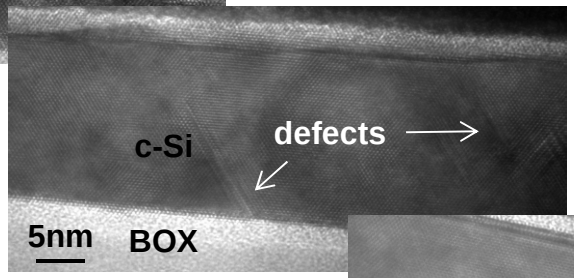


As-implanted

- **Regime II:** Partial epitaxial regrowth

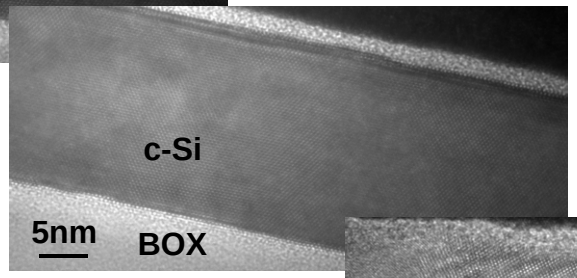


0.60J/cm²



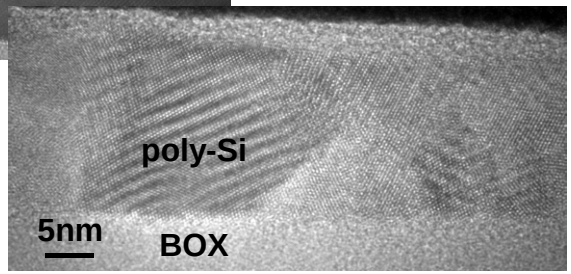
0.75J/cm²

- **Regime III:** Fully monocrystalline, perfectly recrystallized



0.85J/cm²

0.92J/cm²



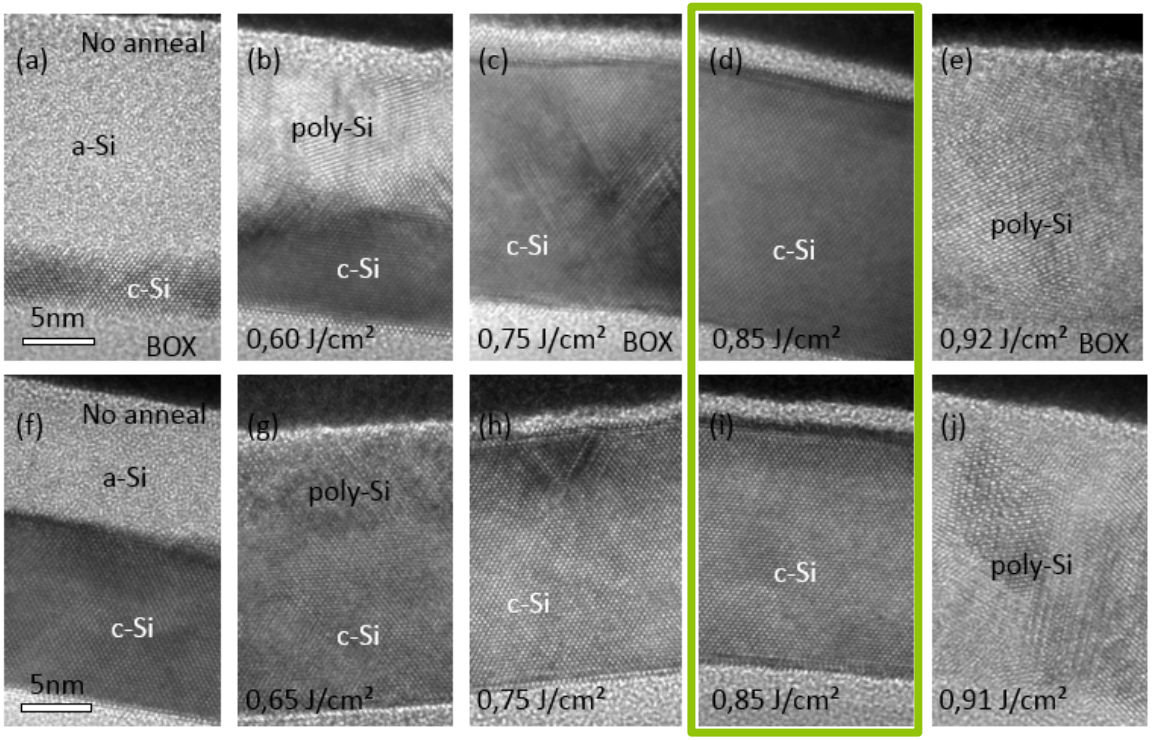
- **Regime (IV):** Poly-Si. SOI layer full melt.

[Kerdiles et al, IWJT 2016]

As & P IMPLANTED SOI: SAME BEHAVIOR UPON UV-NLA

As	14-15 nm a-Si 4-5 nm c-Si
P	8 nm a-Si 12 nm c-Si

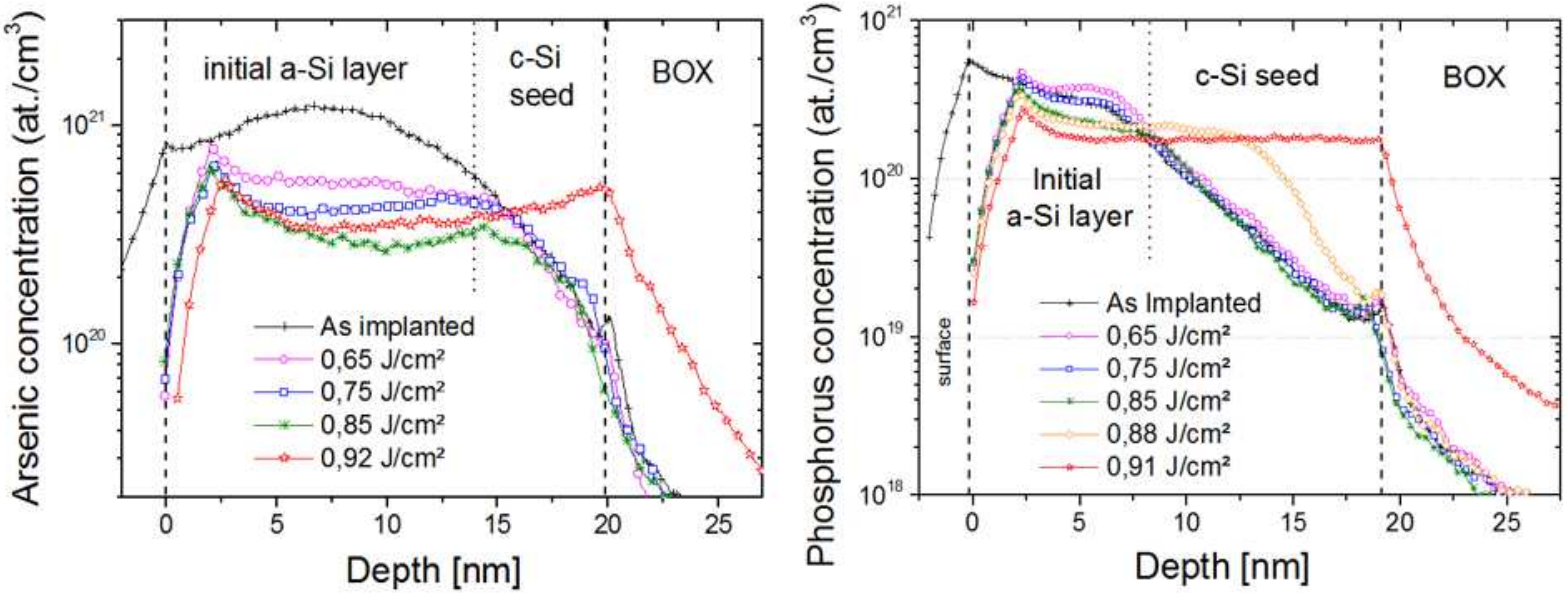
[Acosta et al, IIT 2016]



- Despite different initial amorphizations, similar Rs behavior & TEM observations for the different dopants.

→ **Common process window for dopant activation by UV-NLA**

DOPANT PROFILES (SIMS)



- **Regime II:** Clear dopant redistribution due to the melting of the former a-Si layer
- **Regime III:** Box-like profile extends within the c-Si seed layer
- **Regime IV:** full SOI melting confirmed

→ PAI strategy would allow accurate dopant profile control with a large UV-NLA process window

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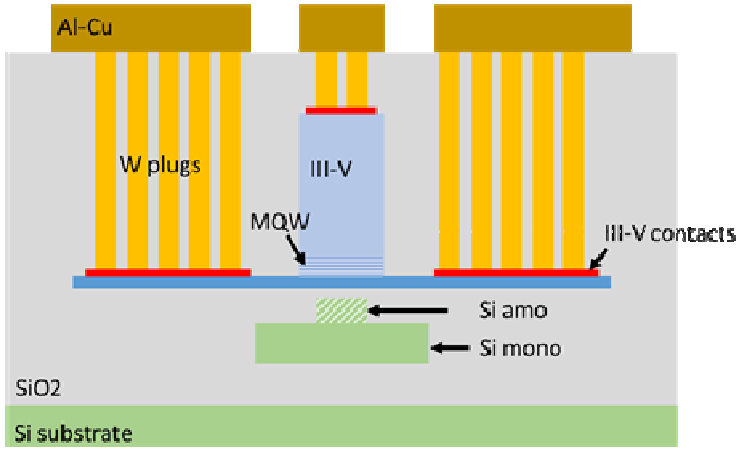
- **More Than Moore : Photonic**

How to manipulate « exotic materials » like silicon and in large diameter substrates

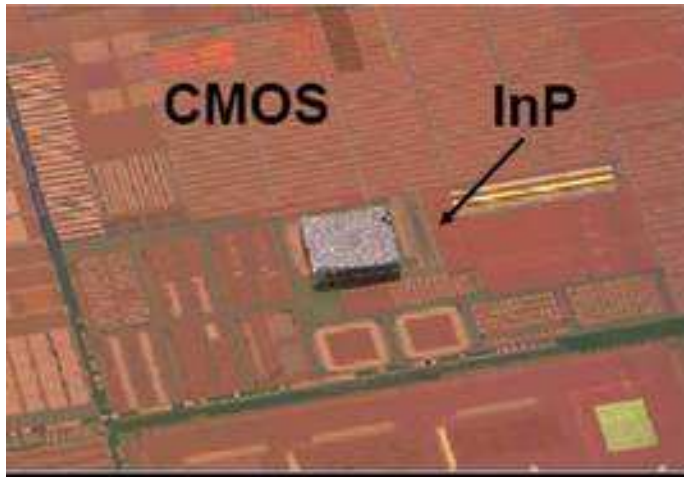
HYBRID III-V/SI LASER – TARGETED PROCESS

Challenges :

- Co-integrate Active (III-V laser) and passive (Si based) components → C2W molecular bonding
- 300mm Si wafers
- CMOS compatible process :
  - No noble metals
  - Conventional patterning steps (no lift off, …)
- Multi-metal level BEOL



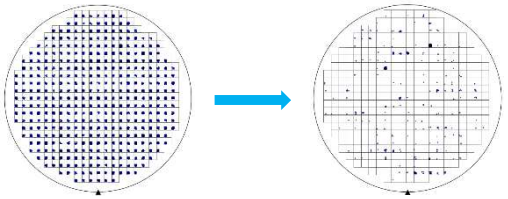
Szelag SPIE 2018



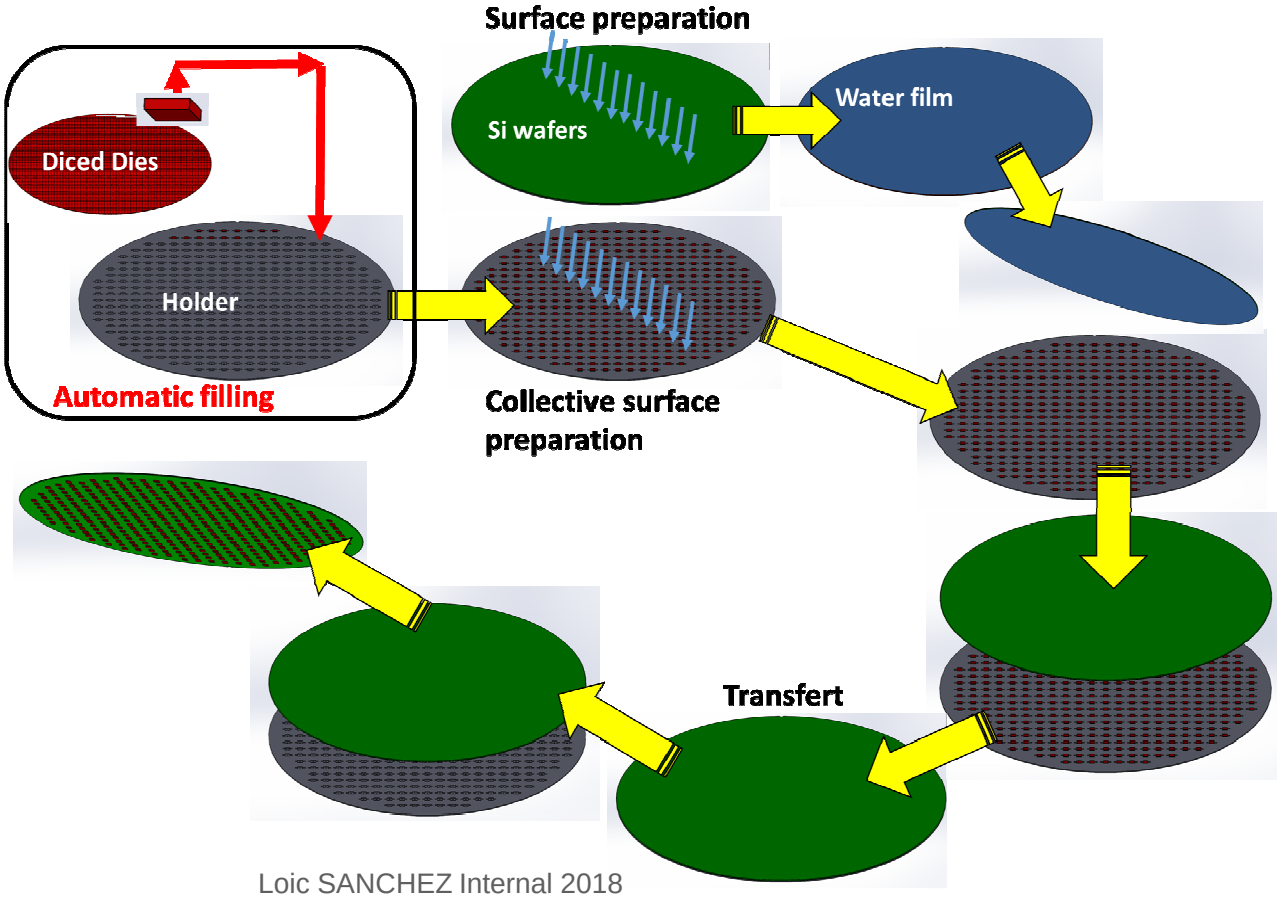
COLLECTIVE DIRECT BONDING OF INP DIES ON SI WAFERS

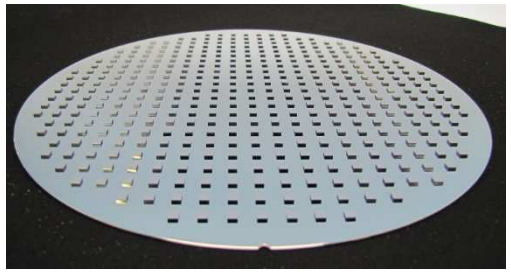
Critical steps:

- Holder fabrication & filling
- Collective surface prep. & characterization
- Transfert by direct bonding & characterization
- Grinding and/or Wet etching of InP substrates



Cleaning of Die/Holder
Defect characterization
(AMAT Complus)

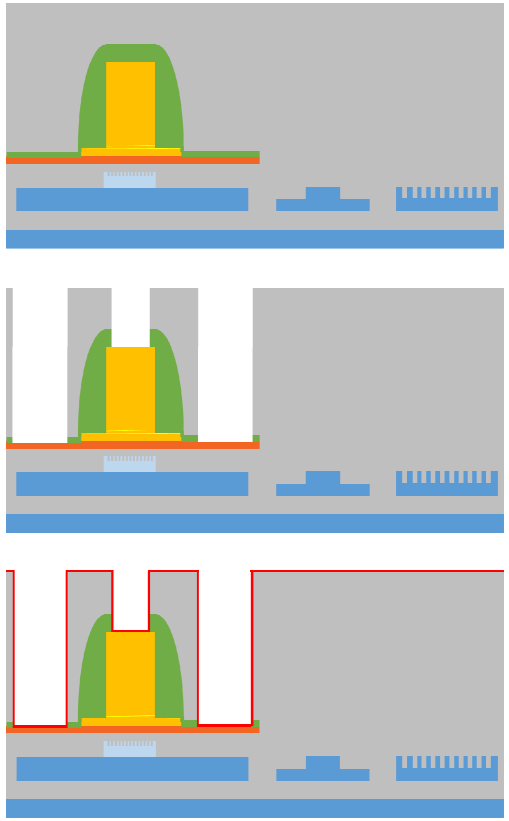




Bonded dies on Si
(3*3mm dies positionned @ +/-150µm)

Loic SANCHEZ Internal 2018

CMOS COMPATIBLE CONTACTS ON III-V MATERIALS



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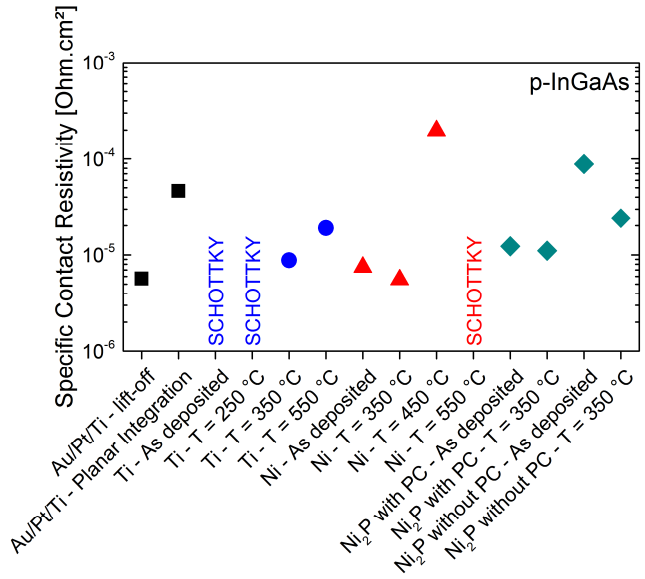
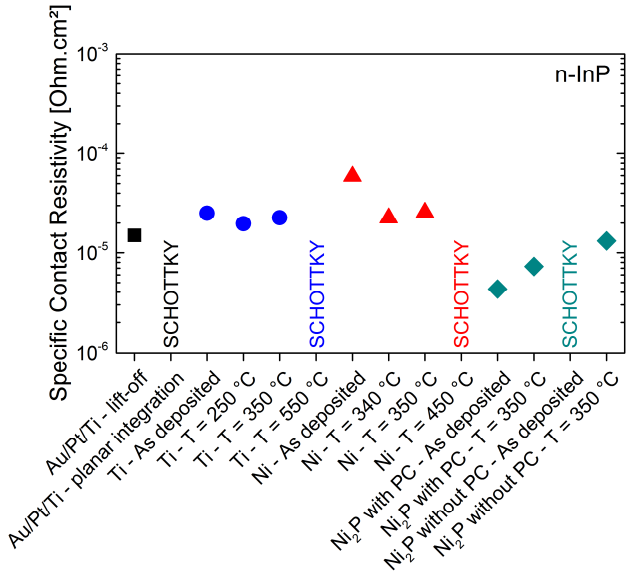
Integration constraint & process cost

→ use the same contact for n-InP and p-InGaAs





NiP with 350℃ annealing for example

- same contact for n-InP and p-InGaAs (Rc < 10E5 Ohm/cm²)

- full CMOS compatible

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A WORLDWILDE ECOSYSTEM ON COMPONENTS

Leti works with a worldwide ecosystem of equipment and material manufacturers to propose solutions based on new architectures (III-V silicon photonic, Cool Cube) and new material integration (III-V, GaN, 2D materials) for IDM, foundries and integrators.

For us, innovative and collective bricks, silicon like process and the use of large diameter substrates are key parameters for early industry adoption

Thank you for your attention